Behzad Ebrahimi

Assistant Professor of Electrical Engineering, Science & Research Branch, Islamic Azad University

https://scholar.google.com/citations?hl=en&user=MCZ0OcMAAAAJ&view_op=list_works&sortby=pubdate

Date of Birth: Nov/17/1983
Marital Status: Married
Military Service Status: Complete the service Military

Contact

E-mail: behzadebrahimielec@gmail.com
bebrahimi2007@gmail.com

Education

Postdoctoral Fellow (Electrical Engineering, Electronics)
University of Tehran, Tehran, Iran, September 2014 until November 2017
Project: **Modeling and design of SRAM with high yield for low power applications and high reliability for high speed applications**
Design of new SRAM structures for augmenting reliability in nanoscale era
(Advisor: Dr. **Afzali-Kusha**)

Ph.D. (Electrical Engineering, Electronics, Nano-technology)
University of Tehran, Tehran, Iran, September 2009 to 2014
GPA 18.7/20.00

Thesis: **Design Optimization of SRAM Cell Using Emerging Si-based Nanoscale Technologies**
(Advisor: Dr. **Afzali-Kusha**)

M.Sc. (Electrical Engineering, Electronics, Semiconductor Devices)
University of Tehran, Tehran, Iran, 2006 to 2009
Total GPA 18.84/20.00

Thesis: **Device Modeling and Optimization of SRAM in Nanoscale era**
(Advisor: Dr. **Afzali-Kusha**)

B.Sc. (Electrical Engineering-Electronics)
University of Tehran, Tehran, Iran, 2001 to 2006
Total GPA 15.14/20.00

Project: **Extraction of SOI Parameters using MINIMOS Simulator**
(Advisor: Dr. **Afzali-Kusha**)

Diploma. (Mathematics and Physics) Shahid Beheshti High School (Administrated by National Organization for Development of Exceptional Students, NODET) Sabzevar, Iran, 1997 to 2000
Total GPA 19.37/20.00

Honor

Computer Architecture & Digital Systems (CADS 2015) best paper award winner (Tehran, Iran), Oct. 2015. Nationwide Outstanding thesis Award from Ministry of Communication and Information Technology, Fava Festival (Tehran, Iran), May 2015. Recognized as exceptional talents. Ranked 1*th* in the entrance exam of the Ph.D. degree in 2009. Ranked 78*th* in the entrance exam of the Iranian universities among 350000 participants in 2001.

Research Interest

- Process variation tolerant design for nano-scaled VLSI circuits
- Low power VLSI design
- Nano-scaled transistors (including FinFET, Tunnel FET transistors) current-voltage characteristics investigation and modeling
- SRAM cell design in nanometer technologies

Publications

ISI International Journal Papers

14- K. Mehrabi, **B. Ebrahimi**, R. Yarmand, A. Afzali-Kusha, and H. Mahmoodi, "Read static noise margin aging model considering SBD and BTI effects for FinFET SRAMs," *Elsevier Microelectronics Reliability*, vol. 65, pp. 20-26, Oct. 2016.

13- **B. Ebrahimi** and M. Asad, "A normally-off fully AlGaN HEMT with high breakdown voltage and figure of merit for power switch applications," *Elsevier Superlattices and Microstructures*, vol. 83, pp. 819-826, Jul. 2015.

12- M. Ansari, H. Afzali-Kusha, **B. Ebrahimi**, Z. Navabi, A. Afzali-Kusha, and M. Pedram, "A Near-Threshold 7T SRAM Cell with High Write and Read Margins and Low Write Time for Sub-20 nm FinFET Technologies," *Elsevier Integration, the VLSI Journal*, vol. 50, pp. 91-106, Jun. 2015.

11- **B. Ebrahimi**, R. Asadpour, A. Afzali-Kusha, and M. Pedram, "A FinFET SRAM cell design with BTI robustness at high supply voltages and high yield at low supply voltages," *Wiley International Journal of Circuit Theory and Applications*, vol. 43, no. 12, pp. 2011-2024, Dec. 2015.

10- **B. Ebrahimi**, A. Afzali-Kusha, and H. Mahmoodi, "Robust FinFET SRAM design based on dynamic back-gate voltage adjustment," *Elsevier Microelectronics Reliability*, vol. 54, no. 11, pp. 2604-2612, Nov. 2014.

9- B. Afzal, **B. Ebrahimi**, A. Afzali-Kusha, and H. Mahmoodi, "An analytical model for read static noise margin including soft oxide breakdown, negative and positive bias temperature instabilities," *Elsevier Microelectronics Reliability*, vol. 53, no. 3, pp. 670-675, Mar. 2013.

8- B. Afzal, **B. Ebrahimi**, A. Afzali-Kusha, and H. Mahmoodi, "Modeling read SNM considering both soft oxide breakdown and negative bias temperature instability," *Elsevier Microelectronics Reliability*, vol. 52, no. 12, pp. 2948-2954, Dec. 2012.

7- B. Afzal, **B. Ebrahimi**, A. Afzali-Kusha, and S. Mohammadi, "Calculation of on-state I-V characteristics of LDMOSFETs based on an accurate LDD resistance modeling," *Elsevier Superlattices and Microstructures*, vol. 52, no. 3, pp. 560-576, Sep. 2012.

6- H. Aghababa, **B. Ebrahimi**, A. Afzali-Kusha, and M. Pedram, "Probability calculation of read failures in nano-scaled SRAM cells under process variations," *Elsevier Microelectronics Reliability*, vol. 52, no. 11, pp. 2805-2811, Nov. 2012.

5- H. Aghababa, **B. Ebrahimi**, M. Saremi, V. Moalemi, and B. Forouzandeh,"G4-FET modeling for circuit simulation by adaptive neuro-fuzzy training systems," *IEICE Electronics Express*, vol. 9, no. 10, pp. 881-887, 2012.

4- **B. Ebrahimi**, B. Afzal, A. Afzali-Kusha, and S. Mohammadi, "A RESURF LDMOSFET with dummy gate on partial SOI," *Springer Journal of the Korean Physical Society*, vol. 60, no. 5, pp. 842-848, Mar. 2012.

3- B. Afzal, **B. Ebrahimi**, A. Afzali-Kusha, and M. Pedram, "An accurate analytical I-V model for sub-90-nm MOSFETs and its application to read SNM modeling," *Springer Journal of Zhejiang University-SCIENCE C (Computers & Electronics)*, vol. 13, no. 1, pp. 58-70, Jan. 2012.

2- M. Saremi, **B. Ebrahimi**, A. Afzali-Kusha, and S. Mohammadi, "A partial-SOI LDMOSFET with triangular buried-oxide for breakdown voltage improvement," *Elsevier Microelectronics Reliability*, vol. 51, no. 12, pp. 2069-2076, Dec. 2011.

1- B. Ebrahimi, M. Rostami, A. Afzali-Kusha, and M. Pedram, "Statistical design optimization of FinFET SRAM using back-gate voltage," *IEEE Trans. on VLSI Systems*, vol. 19, no. 10, pp. 1911-1916, Oct. 2011.

IEEE International Conference Papers

17- K. Mehrabi, **B. Ebrahimi**, and A. Afzali-Kusha, "A Robust And Low Power 7 transistors SRAM Cell Design," *Proc. of the International Symposium on Computer Architecture & Digital Systems,* Oct. 2015, pp. 1-6 **(Best Paper Award)**.

16- R. Yarmand, **B. Ebrahimi**, H. Afzali-Kusha, A. Afzali-Kusha, and M. Pedram, "High Performance and High Yield 5 nm Underlapped FinFET SRAM Design Using P type Access Transistors," *Proc. of the International Symposium on Quality Electronic Design,* Mar. 2015, pp. 10-17.

15- **B. Ebrahimi**, A. Afzali-Kusha and N. Sehatbakhsh, "Robust Polysilicon Gate FinFET SRAM Design using Dynamic Back-Gate Bias," *Proc. of the International conference on Design & Technology of Integrated Systems in nanoscale era,* Mar. 2013, pp. 208-209.

14- **B. Ebrahimi** and A. Afzali-Kusha, "Analysis of SRAM Cell Characteristics Based on High-k Metal-Gate Strained Si/Si1-xGex MOSFET with Consideration of NBTI/PBTI," *Proc. of the International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design,* Sep. 2012, pp. 137-140.

13- **B. Ebrahimi**, H. Afzali-Kusha, and A. Afzali-Kusha, "Low Power and Robust 8T/10T Subthreshold SRAM Cells," *Proc. of the International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design,* Sep. 2012, pp. 141-144.

12- **B. Ebrahimi**, R. Asadpour, and A. Afzali-Kusha, "Low-Power and Robust SRAM Cells Based on Asymmetric FinFET Structures," *Proc. of the Asia Symposium on Quality Electronic Design,* Jul. 2012, pp. 41-46.

11- M. Saremi, **B. Ebrahimi**, and A. Afzali-Kusha, "Ground plane SOI MOSFET based SRAM with consideration of process variation," *Proc. of the IEEE International Conference on Electron Devices and Solid-State Circuits,* Dec. 2010, pp. 1-4.

10- **B. Ebrahimi**, H. Aghababa, and A. Afzali-Kusha, "Analytical modeling of read stability metric of SRAM cell in nanoscale era," *Proc. of the IEEE International Conference on Electron Devices and Solid-State Circuits,* Dec. 2010, pp. 1-4.

9- M. Saremi, **B. Ebrahimi**, A. Afzali-Kusha, and M. Saremi, "Process variation study of ground plane SOI MOSFET," *Proc. of the Asia Symposium on Quality Electronic Design,* Aug. 2010, pp. 66-69.

8- **B. Ebrahimi** and A. Afzali-Kusha, "Realistic CNFET based SRAM cell design for better write stability," *Proc. of the Asia Symposium on Quality Electronic Design,* Jul. 2009, pp. 14-18.

7- A. Ahmadimehr, **B. Ebrahimi**, and A. Afzali-Kusha, "A high speed subthreshold SRAM cell design," *Proc. of the Asia Symposium on Quality Electronic Design,* Jul. 2009, pp. 9-13.

6- **B. Ebrahimi** and A. Afzali-Kusha, "NBTI tolerant 4T double-gate SRAM design," *Proc. Of the Int'l Conference on Ultimate Integration of Silicon,* Mar. 2009, pp. 221-224.

5- S. Zeinolabedinzadeh, **B. Ebrahimi**, and A. Afzali-Kusha, "*Vth*-control method in double gate field effect transistor domino circuits," *Proc. Of the Int'l Conference on Ultimate Integration of Silicon,* Mar. 2009, pp. 297-300.

4- M.Moradinasab, **B. Ebrahimi**, and M. Fathipour, "A compact physical model for subthreshold current in nanoscale FD/SOI MOSFETs," *Proc. Of the Int'l Conference on Ultimate Integration of Silicon,* Mar. 2009, pp. 321-324.

3- F. Jazayeri, S. Soleimani-Amiri, **B. Ebrahimi**, B. Forouzandeh, H-R. Ahmadi, and F. Raissi, "Pseudo-linear automatic gain control system based on nanoscale field effect diode and SOI-MOSFET," *Proc. Of the International Design and Test Workshop*, Dec. 2008, pp. 154-158.

2- **B. Ebrahimi**, S. Zeinolabedinzadeh, and A. Afzali-Kusha, "Low power and robust FinFET based SRAM design," *Proc. Of the IEEE Computer Society Annual Symposium on VLSI,* Apr. 2008, pp. 185-190.

1- M. Rostami, **B. Ebrahimi**, and A. Afzali-Kusha, "Design centering scheme for robust SRAM cell design," *Proc. Of the International Conference on Computer and Communication Engineering,* May 2008, pp. 871-877.

Other Conference Publications

22- **B. Ebrahimi** and A. Afzali-Kusha, "FinFET SRAM Design using Dynamic Back-Gate Bias," *Proc. Of the Nanotechnology Student Conference*, May 2013.

21- R. Asadpour, **B. Ebrahimi,** and A. Afzali-Kusha, "Robust SRAM Cells Based on Asymmetric Nanoscale FinFET," *Proc. Of the Nanotechnology Student Conference*, May 2013.

20- M.Moradinasab, **B.Ebrahimi**, M. Fathipour, and B. Foroozandeh "A compact physical model for subthreshold current in nanoscale FD/SOI MOSFETs," *Proc. Of the International Conference on Electronic Materials*, Jul. 2008, pp. 1109.

19- **B. Ebrahimi** and A. Afzali-Kusha, "double gate based SRAM design using back gate voltage," *Proc. Of the Nanotechnology Student Conference*, Oct. 2008.

18- H. Hosseinzadegan, M. Moradinasab, **B. Ebrahimi**, A. Afzali-Kusha, and E. Arzi, "Deriving a compact model for current-voltage in carbon nanotube field effect transistors in their subthreshold regime," in *Proceedings of the Iran Physics Conference*, Aug. 2007.

Completed Projects

- Compact modeling and optimization of nano-scaled transistors
- SRAM cell design in nano-scale era
- LDMOSFET modeling and optimization

Summary of Qualifications

- In depth practical experience with application packages such as
  Circuit Simulators: HSPICE
- Device and Fabrication Simulators
- Mathematical Software: MATLAB, MAPLE

Teaching

- **CMOS Integrated Circuit Design**-Sadra
- **Electronic Circuits1**- SRBIAU
- **Electronics Lab**-SRBIAU
- **Fundamental of Electrical Circuits Lab**-SRBIAU
- **VLSI**-SRBIAU, USC
- **Advanced Digital Electronics**-SRBIAU, USC
- **Low Power Digital Integrated Circuits**-SRBIAU

Scientific Talks

- FinFET SRAM Design using Dynamic Back-Gate Bias in "Nanotchnology student conference" – May 2013.
- Robust SRAM Cells Based on Asymmetric Nanoscale FinFET in "Nanotchnology student conference" – May 2013.
- Analysis of SRAM Cell Characteristics Based on High-*k* Metal-Gate Strained Si/Si1-*x*Ge*x* MOSFET with Consideration of NBTI/PBTI in "International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design 2012, Spain"-Sep. 2012.
- Low Power and Robust 8T/10T Subthreshold SRAM Cells in "International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design 2012, Spain"-Sep. 2012.
- Realistic CNFET Based SRAM Cell Design for Better Write Stability in "Asia Symposium on Quality Electronic Design ASQED 2009, Malaysia" - Jul. 2009.
- A High Speed Subthreshold SRAM Cell Design in "ASQED 2009, Malaysia" -Jul. 2009
- Double Gate Based SRAM Design Using Back Gate voltage in "Nanotchnology student conference" – Oct. 2008.